

# EE366: CMOS VLSI Design

Spring 2009

- ❑ **Instructor:**
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  - ❑ **Office Hours:** MW 2:30-3:45
- ❑ **Time and Place:**
  - ❑ **Lecture:** MWF 1:30 – 2:20 PM , Holmes Hall 242
  - ❑ **Lab:** Thursday 9:00 – 11:50 AM, Holmes Hall 387
- ❑ **Teaching Assistant:**
  - ❑ Ka Hing Chan, kahing@hawaii.edu
  - ❑ office hour: TBD
- ❑ **Class homepage**
  - ❑ <http://www.ee.hawaii.edu/~xrzhou/ee366> **(To be constructed)**
- ❑ **Prerequisite:** Digital design basics (EE 260), basic circuit theory (EE211).
- ❑ **Credits:** 4 – (2 design credits).
  - ❑ Three 1-hour lectures and one 3-hour lab per week
- ❑ **Brief Course Description:** This course provides the electrical & computer engineering student with the analytical and computer skills required for the analysis, computer simulation, design, and computer-aided physical layout of digital integrated circuits. The course is preparatory for study in the field of Very Large Scale Integrated (VLSI) digital circuits and engineering practice.

## ❑ **Course Outcomes**

The following are the course outcomes and the subset of Program Outcomes (numbered 1-11 in square braces "[ ]") they address:

❑ Understand CMOS technology. [1]
❑ Be able to do DC and transient analysis, of digital CMOS circuits. [1,5]
❑ Be able to use a circuit simulator (HSPICE) to perform analysis and optimizations of digital circuits. [3,5,11]
❑ Become proficient in a hardware description language (e.g., VHDL). [3,5,11]
❑ Be able to do design trade-offs considering area, speed, power and reliability. [5]
❑ Be able to estimate area and power dissipation. [5]
❑ Be able to design small ASICs. [3]
❑ Understand logic synthesizers and be able to synthesize a simple circuit. [11]

- ❑ **Textbooks:**
  - ❑ Neil H.E. Weste, David Harris, “CMOS VLSI Design – A circuits and Systems Perspective,” Addison-wesley, **3<sup>nd</sup> ed.** 2004.
  - ❑ Douglas L. Perry, “VHDL – Programming by Example,” McGraw-Hill 2002. (ELECTRONIC VERSION AVAILABLE AT UH MANOA LIBRARY).
- ❑ **Grading Policy:**
  - ❑ Written homework: 15%
  - ❑ Lab reports: 25%
  - ❑ Midterm: 30%
  - ❑ Final exam: 30%
- ❑ **Computer Usage:** Half of the class assignments are designs that require operating a computer skillfully. The CAD tools to be used are installed on a UNIX system.

- ❑ **Homework and Labs:**
  - ❑ Homework and lab reports (7 to 10) are due a week after the homework is assigned or the lab is scheduled. A maximum of 2 delayed homework and labs (at most 1 class day) will be accepted. Homework and labs submitted in excess of the 2nd allowed will be corrected but will not be given credit.
- ❑ **List of topics:**
  1. **CMOS Basics (20 hr)**
    - ❑ Introduction to modern digital design and Technology Trends (1 hr).
    - ❑ Basics of Solid State Physics and MOS Transistors (1½ hr).
    - ❑ Manufacturing Process and Design Rules (1½ hr).
    - ❑ CMOS Logic and elementary design (2 hr).
    - ❑ Types of ASICs and Structured Design (1 hr).
    - ❑ MOS transistor theory (3 hr).
    - ❑ CMOS inverter: DC analysis (1½ hr).
    - ❑ CMOS inverter: transient analysis (1 hr).
    - ❑ MOS SPICE Models and Simulations (½ hr).
    - ❑ Delay estimation (RC and Elmore Delay model) (1 hr).
    - ❑ Delay estimation and Gate sizing (Logical Effort) (2 hr).
    - ❑ Power Dissipation and Low Power Design (1 hr).
    - ❑ Interconnect modeling and wire engineering (2 hr).
    - ❑ Design margin, process variation and Device Scaling (1 hr).
  2. **CMOS VLSI Design (14½ hr)**
    - ❑ CMOS combinational logic – Static, Rationed, Dynamic, Pass-Transistors Families (2 hr).
    - ❑ Sequencing Methods (Static, Two-Phase, Time Borrowing, Clock Skew) (1 hr).
    - ❑ Sequential logic design (2 hr).
    - ❑ Adders: Single-bit circuits (1 hr).
    - ❑ Adders: Ripple, Generation and Propagation, Manchester, Carry Skip (1 hr).
    - ❑ Adders: Look-ahead, Select, Conditional-Sum, Tree (1½ hr).
    - ❑ Other Arithmetic Building Blocks: One-Zero, Comparators, Counters, Shifters (1 hr).
    - ❑ Designing Arithmetic Building Blocks: Multipliers (1 hr).
    - ❑ Array subsystems: SRAM (1 hr).
    - ❑ Array subsystems: DRAM, ROM, CAM, PLA (1 hr).
    - ❑ Power Distribution (IR Drop, di/dt noise) and I/O circuits (1 hr).
    - ❑ Clock generation and Distribution (1 hr).
  3. **Hardware Description Languages (10 hr) (chapters from “VHDL – Programming by Example,” book)**
    - ❑ Hardware description languages: Introduction and Rationale (½ hr).
    - ❑ VHDL: Hands-on (½ hr).
    - ❑ VHDL: Basic Terminology and Design Units (1hr).
    - ❑ VHDL: Behavioral Modelling (1 hr).
    - ❑ VHDL: Process Semantics and Interaction (2 hr).
    - ❑ VHDL: Basic Syntax and Data Types (2 hr).
    - ❑ VHDL: Subprogram and Packages – the std\_logic types (1 hr).
    - ❑ VHDL: Configurations (1 hr).
    - ❑ VHDL and synthesis (1 hr).

**Note on academic honesty:**

**NO PLAGIARISM WILL BE TOLERATED. DISCUSSION ON HOMEWORKS AND LABS IS ENCOURAGED, BUT SUBMITTED WORK IS THE RESPONSIBILITY OF EACH INDIVIDUAL STUDENT.**

